REMARKS

Claims 1 and 3-30 are rejected under 35 U.S.C. 112, first paragraph as containing subject matter which was not described in the specification. The phrase objected to by the Examiner has been deleted because Applicants feel it is not necessary for patentability. Accordingly, deletion of the phrase objected to by the Examiner should not be interpreted as Applicants admitting or agreeing that the deleted phrase is not described in the specification.

Claims 33 and 34 are objected to for lack of antecedent basis. Claims 33 and 34 are amended to depend from claim 32, which supplies the proper antecedent basis.

Applicants respectfully submit that all claims meet the requirements of 35 U.S.C. 112 and request that the Examiner withdraw his rejections under 35 U.S.C. 112.

Claims 1, 3-5, 12-35, and 42-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour et al., U.S. Patent No. 5,926,726 (hereinafter "Bour") in view of Koike et al., U.S. Patent No. 5,811,319 (hereinafter Koike). Applicants respectfully traverse the rejection. Claims 1 and 31 are amended to recite "growing in a chamber a III-V nitride compound semiconductor layer at a first temperature . . . cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process . . . and <u>after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C</u>." Applicants respectfully submit that the combination of Bour and Koike does not teach the above-underlined element of claims 1 and 31.

The Examiner cites two sections of Bour as teaching annealing, column 2, lines 32-64 and column 6, lines 40-65. The passage in column 2 teaches a high temperature, quasi-in-situ anneal according to a process taught by Nakamura:

> Then, an anneal process is carried out after extinguishing the flow of H_2 and NH_3, introducing a N_2 flow, and <u>raising the reactor temperature back up to the growth temperature regime of the GaN film, e.g. 1,000°C</u>, and permitting the anneal to be accomplished for 20 minutes.

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Since the anneal taught in column 2 is performed in the growth temperature regime, the passage in column 2 does not teach "heating said p-type layer to a third temperature greater than the second temperature and less than 625°C" as recited in claims 1 and 31.

It would not have been obvious to modify the anneal taught in column 2 to meet the above-quoted limitation of claims 1 and 31 because at column 2, line 4, Bour recites 700°C as the lower end of acceptable temperatures for the Nakamura anneals described in column 2. As a result, a person of skill in the art would not expect an anneal at a temperature less than 625°C to be hot enough to provide acceptor activation.

The anneal taught in column 6 does not teach "<u>cooling said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process</u> . . . and after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than 625°C" as recited in claims 1 and 31. Rather, the anneal described in column 6 takes place as part of the cool-down process, and does not reheat the device for an anneal after cool-down is complete. Bour states at column 6, lines 39-54:

> Thus, in step 34, the reactor 10 is cooled down to a temperature where surface decomposition of as-grown p-type GaN layer 22 will not further occur, such as may be in the range of around 600°C to 800°C. . . . Upon attainment of this temperature, the N outdiffusion preventor gas, NH_3, is switched out of reactor 10, as shown in step 35 of Fig. 6, and acceptor activation is performed either as the reactor is further cooled down or at a temperature maintained for a given period of time as indicated at step 36. As an example, if the temperature is maintained at 600°C, then the time period for activation may be tens of minutes, such as, for example, between about 20 to about 40 minutes.

Since Bour's anneal in column 6 is performed as part of cool-down, not after cool-down is complete, Bour's anneal in column 6 does not cool the acceptor-doped layer to a second temperature, then heat the p-type layer to a third temperature greater than the second temperature as recited in claims 1 and 31. It would not have been obvious to modify Bour's column 6 anneal to do so, because Bour teaches that it is undesirable to complete cool-down prior to performing an anneal. See, for example, column 3, lines 46-50, which states that the

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problems associated with such an anneal include high processing costs, and potential contamination from exposure to the atmosphere accompanying ex-situ processing. Even if the post-cool-down anneal is performed in situ, a person of skill in the art would still expect to encounter high processing times and costs and potential contamination, and would therefore not be motivated to modify Bour's column 6 anneal.

Neither of the anneals taught by Bour teach all the elements of claims 1 and 31, nor would it be obvious to modify either anneal to match the process taught in claims 1 and 31. Koike was cited in reference to different elements of claims 1 and 31 and adds nothing to Bour with respect to the deficiencies in Bour's anneals. Accordingly, Applicants respectfully submit that claims 1 and 31 distinguish over the combination of Bour and Koike and are therefore allowable. Claims 3-5 and 12-30 depend from claim 1 and are therefore allowable for at least the same reason. Claims 32-35 and 42-60 depend from claim 31 and are therefore allowable for at least the same reason.

Claims 6, 9, 11, 36, 39, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour and Koike as applied to claim 1, further in view of Takatani, U.S. Patent No. 6,100,174. Claims 6, 9, and 11 depend from claim 1 and are therefore allowable for at least the reasons stated above for claim 1. Claims 36, 39, and 41 depend from claim 31 and are therefore allowable for at least the reasons stated above for claim 31. Takakani adds nothing to the deficiencies of Bour and Koike with respect to claims 1 and 31. Accordingly, claims 6, 9, 11, 36, 39, and 41 are allowable over the combination of Bour, Koike, and Takatani.

Claims 10 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour, Koike, and Takatani, as applied to claim 9, and further in view of Peng et al., U.S. Patent No. 5,895,223. Claim 10 depends from claim 9, which depends from claim 1. Claim 10 is therefore allowable for at least the reasons stated above for claim 1. Claim 50 depends

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from claim 31 and are therefore allowable for at least the reasons stated above for claim 31. Takakani and Peng et al. add nothing to the deficiencies of Bour and Koike with respect to claims 1 and 31. Accordingly, claims 10 and 50 are allowable over the combination of Bour, Koike, Takatani, and Peng et al.

Claims 13 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour and Koike as applied to claim 5, further in view of Peng et al. Claim 13 depends from claim 5, which depends from claim 1. Claim 13 is therefore allowable for at least the reasons stated above for claim 1. Claim 43 depends from claim 35, which depends from claim 31. Claim 43 is therefore allowable for at least the reasons stated above for claim 31. Peng et al. adds nothing to the deficiencies of Bour and Koike with respect to claims 1 and 31. Accordingly, claims 13 and 43 are allowable over the combination of Bour, Koike, and Peng et al.

Claims 7, 8, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bour and Koike as applied to claim 5, further in view of Nitta et al., U.S. Patent No. 5,789,265. Claims 7 and 8 depend from claim 5, which depends from claim 1. Claims 7 and 8 are therefore allowable for at least the reasons stated above for claim 1. Claims 37 and 38 depend from claim 35, which depends from claim 31. Claims 37 and 38 are therefore allowable for at least the reasons stated above for claim 31. Nitta et al. adds nothing to the deficiencies of Bour and Koike with respect to claims 1 and 31. Accordingly, claims 7, 8, 37, and 38 are allowable over the combination of Bour, Koike, and Nitta et al.

In view of the above arguments, Applicants respectfully request allowance of all

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pending claims. Should the Examiner have any questions, the Examiner is invited to call the undersigned at (408) 382-0480.

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Respectfully submitted,

R Leiterman

Rachel V. Leiterman
Attorney for Applicants
Reg. No. 46,868

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SUITE 223
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(408) 382-0480
FAX (408) 382-0481

ATTACHMENT A

IN THE CLAIMS

The claims are amended as follows:

1. (Twice Amended) A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen passivates at least some of said acceptor impurities;

[lowering] <u>cooling</u> said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process;

preventing additional hydrogen from diffusing into said acceptor-doped layer substantially [throughout] <u>during</u> the [entire] cool-down process;

causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

<u>after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than</u> [annealing said p-type layer at a temperature below] 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

31. (Amended) A method for manufacturing a p-type III-V nitride compound semiconductor comprising:

growing in a chamber a III-V nitride compound semiconductor layer at a first temperature while introducing acceptor impurities into said layer to form an acceptor-doped layer, said chamber containing one or more gases providing hydrogen such that said hydrogen

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passivates at least some of said acceptor impurities;

[lowering] <u>cooling</u> said acceptor-doped layer to a second temperature significantly lower than said first temperature during a cool-down process, thereby causing said acceptor-doped layer to be a p-type layer, having p-type conductivity and a hole density between approximately $3x10^{15}cm^{-3}$ and $1x10^{18}cm^{-3}$, after said cool-down process; and

<u>after said cooling, heating said p-type layer to a third temperature greater than the second temperature and less than</u> [annealing said p-type layer at a temperature below] 625°C to remove hydrogen from said p-type layer thereby increasing said hole density and lowering the resistivity of said p-type layer.

33. (Amended) The method of Claim [31] <u>32</u> wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises preventing gases containing hydrogen from entering said chamber during said cool-down process and removing hydrogen in said chamber during said cool-down process.

34. (Amended) The method of Claim [31] <u>32</u> wherein said preventing additional hydrogen from diffusing into said acceptor-doped layer comprises forming an n-type semiconductor layer cap over said acceptor-doped layer prior to said cool-down process.

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